Abstract

A signal processor has a plurality of channels, each channel configured to receive an input signal stream, to reduce the signal to a direct current signal and to process the signal according to the stream signal. Each channel also has a plurality of low pass filters configured to filter in-phase and quadrature-phase modulator outputs with a first low pass filter and to filter a reference quadrature signals, and a gain control configured to re-modulate gain adjusted output signals with the filtered quadrature signals. The processor further includes an inverter to invert the in-phase filtered reference signal and means to multiply the quadrature gain adjusted output signal.